

WHAT IS CLAIMED IS:

- 1 1. A semiconductor device comprising:
2 a substrate;
3 a first interlayer dielectric located on the substrate;
4 a connection node located in the first interlayer dielectric in a first region;
5 a second interlayer dielectric located on the first interlayer dielectric;
6 an integrated capacitor having a top electrode and a bottom electrode formed in the
7 second interlayer dielectric such that the bottom electrode is in electrical contact with the
8 connection node; and
9 a connection node contact positioned through the second interlayer dielectric providing
10 an electrical connection to the connection node.
- 1 2. The semiconductor device of claim 1, wherein a DRAM cell is located in a second region
2 of the substrate.
- 1 3. The semiconductor device of claim 2, wherein the DRAM cell comprises a transistor
2 located on the substrate and a storage capacitor positioned in the second interlayer dielectric.
- 1 4. The semiconductor device of claim 3, wherein a bottom electrode of the storage capacitor
2 is in electrical contact with a source/drain region of the transistor.
- 1 5. The semiconductor device of claim 4, wherein the connection node and a device contact
2 in the first interlayer dielectric are made of a first material, the device contact electrically

3 connecting the bottom electrode of the storage capacitor and the source/drain region of the
4 transistor.

1 6. The semiconductor device of claim 5, wherein the first material is a material selected
2 from the group consisting of a metal, an elemental metal, a transition metal, and a combination
3 thereof.

1 7. The semiconductor device of claim 3, wherein the connection node and a gate of the
2 transistor are made of a first material.

1 8. The semiconductor device of claim 7, wherein the first material is polysilicon.

1 9. The semiconductor device of claim 1, wherein the bottom electrode of the integrated
2 capacitor is in electrical contact with the connection node via a second connection node contact.

1 10. A semiconductor device comprising:
2 a connection node located on a substrate in a first region;
3 a first interlayer dielectric located on the connection node;
4 a second interlayer dielectric located on the first interlayer dielectric;
5 an integrated capacitor having a top electrode and a bottom electrode formed in the
6 second interlayer dielectric;
7 a first connection node contact formed through the first interlayer dielectric electrically
8 coupling the bottom electrode to the connection node; and
9 a second connection node contact formed through the first interlayer dielectric providing
10 an electrical connection to the connection node.

1 11. The semiconductor device of claim 10, wherein a first device is located on a second
2 region of the substrate.

1 12. The semiconductor device of claim 11, wherein a first device is a DRAM cell.

1 13. The semiconductor device of claim 12, wherein the DRAM cell comprises a transistor
2 located on the substrate and a storage capacitor located in the second interlayer dielectric.

1 14. The semiconductor device of claim 13, wherein a bottom electrode of the storage
2 capacitor is in electrical contact with a source/drain region of the transistor.

1 15. The semiconductor device of claim 13, wherein the connection node and a gate of the
2 transistor are made of a first material.

- 1 16. The semiconductor device of claim 15, wherein the first material is polysilicon.
- 1 17. The semiconductor device of claim 11, wherein the first device is a logic device.
- 1 18. The semiconductor device of claim 17, wherein the logic device comprises a transistor
2 located on the substrate.
- 1 19. The semiconductor device of claim 18, wherein the connection node and a gate of the
2 transistor are made of a first material.
- 1 20. The semiconductor device of claim 19, wherein the first material is polysilicon.
- 1 21. The semiconductor device of claim 18, further comprising a transistor contact positioned
2 through the first interlayer dielectric providing an electrical connection to the transistor.
- 1 22. The semiconductor device of claim 21, wherein the first connection node contact and the
2 transistor contact are formed of a material selected from the group consisting of a metal, an
3 elemental metal, a transition metal, and a combination thereof.
- 1 23. The semiconductor device of claim 21, wherein the first connection node contact and the
2 transistor contact include a barrier layer.
- 1 24. The semiconductor device of claim 23, wherein the barrier layer is formed of a material
2 selected from the group consisting of titanium, titanium nitride, and combinations thereof.

- 1 25. The semiconductor device of claim 10, wherein a surface of the connection node is
- 2 silicided.

1 26. A method of forming a semiconductor device, the method comprising:
2 providing a substrate;
3 forming a first interlayer dielectric on the substrate;
4 forming a connection node located in the first interlayer dielectric in a first region;
5 forming a second interlayer dielectric on the first interlayer dielectric;
6 forming an integrated capacitor having a first top electrode and a first bottom electrode
7 formed in the second interlayer dielectric such that the first bottom electrode is in electrical
8 contact with the connection node; and
9 forming a connection node contact through the second interlayer dielectric providing an
10 electrical connection to the connection node.

1 27. The method of claim 26, further comprising forming a device on a second region of the
2 substrate before forming the first interlayer dielectric.

1 28. The method of claim 27, wherein the device is a transistor.

1 29. The method of claim 28, further comprising simultaneously forming a contact in the first
2 interlayer dielectric when the step of forming a connection node is performed, wherein the
3 contact is electrically connected to the transistor.

1 30. The method of claim 29, further comprising simultaneously forming a storage capacitor
2 in the second interlayer dielectric when the step of forming the integrated capacitor is performed,
3 wherein the storage capacitor has a second top electrode and a second bottom electrode formed
4 such that the second bottom electrode is in electrical contact with the transistor via the contact.

1 31. The method of claim 29, wherein the connection node and the contact are formed of a
2 first material.

1 32. The method of claim 31, wherein the first material is a material selected from the group
2 consisting of a metal, an elemental metal, a transition metal, and a combination thereof.

1 33. The method of claim 28, wherein the connection node and a gate electrode of the device
2 are formed of a first material.

1 34. The method of claim 33, wherein the first material is polysilicon.

1 35. The method of claim 26, further comprising forming a second connection node contact
2 electrically coupling the first bottom electrode to the connection node.

1 36. A method of forming a semiconductor device, the method comprising:
2 providing a substrate having at least one first region and one second region;
3 forming a transistor on the first region;
4 forming a first interlayer dielectric over the substrate;
5 forming a connection node in the first interlayer dielectric upon the second region, the
6 connection node being a thickness substantially equivalent to the thickness of the first interlayer
7 dielectric;
8 forming a second interlayer dielectric on the first interlayer dielectric;
9 forming an integrated capacitor in the second interlayer dielectric upon the second region
10 and a storage capacitor in the second interlayer dielectric upon the first region, the integrated
11 capacitor having a first bottom electrode being in electrical contact with the connection node and
12 the storage capacitor having a second bottom electrode, the second bottom electrode being in
13 electrical contact with the transistor; and
14 forming a connection node contact in the second dielectric layer, the connection node
15 contact being in electrical contact with the connection node.

1 37. The method of claim 36, further comprising simultaneously forming a transistor contact
2 in the first interlayer dielectric when the step of forming the connection node is performed,
3 wherein the transistor contact electrically connects a source/drain of the transistor with the
4 second bottom electrode.

1 38. The method of claim 37, wherein the transistor contact and the connection node are
2 formed of a first material.

1 39. The method of claim 38, wherein the first material is a material selected from the group
2 consisting of a metal, an elemental metal, a transition metal, and a combination thereof.

1 40. The method of claim 36, wherein the connection node is formed of a material selected
2 from the group consisting of a metal, an elemental metal, a transition metal, and a combination
3 thereof.

1 41. The method of claim 36, wherein forming the connection node includes forming a barrier
2 layer on the first interlayer dielectric and forming a conductive layer on the barrier layer.

1 42. The method of claim 41, wherein the barrier layer is formed of a material selected from
2 the group consisting of titanium, titanium nitride, and combinations thereof.

1 43. The method of claim 41, wherein the conductive layer comprises tungsten.

1 44. A method of forming a semiconductor device, the method comprising:
2 providing a substrate having at least one first region and at least one second region;
3 forming a transistor on the first region and a conductive layer on the second region ;
4 forming a first interlayer dielectric located on the substrate and covering the transistor
5 and the conductive layer;
6 forming a first connection node contact to the conductive layer through the first interlayer
7 dielectric;
8 forming a second interlayer dielectric on the first interlayer dielectric; and
9 forming a capacitor in the second interlayer dielectric, the capacitor having a first bottom
10 electrode and a first top electrode, the first bottom electrode being in electrical contact with the
11 first connection node contact.

1 45. The method of claim 44, wherein the conductive layer is polysilicon.

1 46. The method of claim 44, further comprising simultaneously forming a transistor contact
2 in the first interlayer dielectric when the step of forming the first connection node contact is
3 performed, wherein the transistor contact electrically connects to the transistor through the first
4 interlayer dielectric.

1 47. The method of claim 46, wherein the first connection node contact and the transistor
2 contact are formed of the same material.

1 48. The method of claim 47, wherein the first connection node contact and the transistor
2 contact are formed of a material selected from the group consisting of a metal, an elemental
3 metal, a transition metal, and a combination thereof.

1 49. The method of claim 44, wherein forming the first connection node contact includes
2 forming a barrier layer on the first interlayer dielectric and forming a conductive liner on the
3 barrier layer.

1 50. The method of claim 49, wherein the barrier layer is formed of a material selected from
2 the group consisting essentially of titanium, titanium nitride, and combinations thereof.

1 51. The method of claim 49, wherein the conductive liner comprises tungsten.

1 52. The method of claim 44, wherein a surface of the conductive layer is silicided.

1 53. A semiconductor device comprising:
2 a transistor and a connection node located on the substrate;
3 a first interlayer dielectric blanketed on the substrate covering the transistor and the
4 connection node;
5 a second interlayer dielectric blanketed on the first interlayer dielectric;
6 an integrated capacitor having a first top electrode and a first bottom electrode located in
7 the second interlayer dielectric;
8 a storage capacitor having a second top electrode and a second bottom electrode located
9 in the second interlayer dielectric;
10 a first connection node contact located through the first interlayer dielectric electrically
11 coupling the first bottom electrode to the connection node;
12 a second connection node contact formed through the first interlayer dielectric providing
13 an electrical connection to the connection node; and
14 a transistor contact formed through the first interlayer dielectric electrically coupling the
15 second bottom electrode to a source/drain region of the transistor.

1 54. The semiconductor device of claim 53, wherein the first connection node contact, the
2 second connection node contact and the transistor contact are made of a material selected from
3 the group consisting of a metal, an elemental metal, a transition metal, and a combination
4 thereof.

1 55. The semiconductor device of claim 53, wherein the first connection node contact, the
2 second connection node contact and the transistor contact include a barrier layer.

1 56. The semiconductor device of claim 55, wherein the barrier layer is made of a material
2 selected from the group consisting of titanium, titanium nitride, and combinations thereof.

1 57. The semiconductor device of claim 55, wherein the surface of the first and second
2 connection contact node is silicided.